Anjuman Islam Janjira Degree College of Science Murud-Janjira, Raigad-402401 Affiliated to University of Mumbai	
Class: -F.Y.B.Sc. (C.S)	**Subject: - : Digital Systems & Architecture**
Semester:- I Additional Exam	**Vertical:- Major(MJ1)**
Exam Event:- (FH) Summer 2026	**Marks: - 30**
Date: - 24/02/2026	**Duration: - 01:00 Hour**

N.B. – 1 – All questions are compulsory.
2 – All questions have internal choice.
3 – Figures to the right indicate full marks.

Q1. Answer the following question. (Any 2 out of 4) **10**

1) Write concept of full adder along with truth table and circuit diagram.
2) Create a circuit diagram for the expression Y=(A+C).(AD+AD')+AC+C.
3) Define CPU and describe its components with functions.
4) Compare between computer organization and computer architecture.

Q2. Answer the following question. (Any 2 out of 4) **10**

1) List down the features of RAID levels.
2) Define the term: a)Principle of Locality b)Cache Performance.
3) Write a note on page replacement algorithm.
4) Illustrate the memory hierarchy with detail.

Q3. Answer the following question. (Any 2 out of 4) **10**

1) Explain de-multiplexer in detail.
2) Define truth table and what is logic gate? Classify the logic gate in detail.
3) Find out page fault for the reference string using LRU and FIFO method for 3-page frames:6 0 12 0 30 4 2 32 1 20 15.
4) Comparison between CISC and RISC.